REMARKS

Claims 1-47 are pending in the present application. Claims 1-9, 20-23, 25, 27-28, 36, 38-39, and 46-47 were cancelled. Claims 24, 26, 32, 35, 37, and 43 were amended. Accordingly, claims 10-19, 24, 26, 29-35, 37, 40-45 are now pending in the application.

The Examiner indicated that claims 17, 28, 32-34, 39, and 43-45 are objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including the limitations of the base claim and any intervening claims. Applicant has amended claim 24 to include limitations similar to the limitations recited in claims 25, 27, and 28. Applicant has also amended claim 32 to include limitations similar to the limitations recited in claims 24 and 29. Applicant has amended claim 35 include limitations similar to the limitations recited in claims 36, 38, and 39. Applicant has amended claims 43 to include limitations similar to the limitations recited in claims 35 and 40. Accordingly, Applicant submits that claims 24, 32, 35, and 43, along with their respective dependent claims to patentably distinguish over the cited art. Applicant has not, at this juncture, rewritten claim 17 into independent form.

Claims 1, 4-10, 13-16, 18-27, 29-31, 35-38, 40-42, and 46-47 stand rejected under 35 U.S.C. §102(e) as being anticipated by Forsman et al. (U.S. Patent Number 6,742,139) (hereinafter 'Forsman'). Applicant respectfully traverses portions of this rejection.

Claims 2-3, and 11-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Forsman in view of Dziadosz et al. (U.S. Patent Number 5,832,222) (hereinafter 'Dziadosz'). Applicant respectfully traverses portions of this rejection.

Applicant's claim 10 recites a computer system comprising, in pertinent part,

"a plurality of **system** controllers, each comprising:
a processor;
a memory; and

a plurality of input/output (I/O) controllers each configurable with a plurality of I/O connections to another of the plurality of system controllers, wherein each of the plurality of I/O controllers is further configurable with an I/O connection to each of one or more sensors;

wherein the plurality of system controllers includes **a primary system controller and a secondary system controller**;

one or more processors;...

wherein the primary system controller is configured to configure the one or more processors, the one or more memories, and the one or more I/O devices into one or more domains,

wherein the primary system controller is further configured to update secondary system controller with a system configuration."

The Examiner asserts that Forsman teaches each and every limitation recited in Applicant's claim 10. Applicant respectfully disagrees with the Examiner's assertion and his characterization of Forsman. Specifically, Forsman discloses at col. 1, lines 12-16

> "Some systems, such as the RS/6000, a product of the International Business Machines Corporation of Armonk, N.Y., offer **a** service processor that is a shared resource within the data processing system. The service processor provides vital monitoring to the operating system. However, in existing systems, if the **host** operating system experiences a communication failure with the service processor, there is no recovery mechanism for the host to recover communications with the service processor."

Forsman also discloses at col. 2, lines 32-35

> "The present invention provides a method, system, and apparatus for reestablishing communications between a host and a service processor after the service processor has ceased to function correctly."

Forsman futher discloses at FIG. 1 and at col. 2 lines 10-65

> "Data processing system 100 may be a symmetric multiprocessor (SMP) system including a plurality of processors 101, 102, 103, and 104 connected to system bus 106... PCI host bridge 130 provides an interface for a PCI bus 131 to connect to I/O bus 112. Service processor 135 is coupled to PCI Host Bridge 130 through PCI Bus 131... When data processing system 100 is initially powered up, service processor 135 uses the JTAG/I.sup.2 C buses 132, 134, and 136 to interrogate the system (Host) processors 101-104..."

From the foregoing, Forsman clearly teaches a plurality of host processors and **one** service processor for monitoring the system. Applicant notes that the service

processor of Forsman may be analogous in some ways to the Applicant's system controller, and the host processors of Forsman may be analogous in some ways to the Applicant's one or more processors.

Thus, Forsman **does not teach or disclose** "a plurality of **system** controllers" as recited in Applicant's claim 10. Forsman also **does not teach or disclose** "wherein the plurality of system controllers includes a primary system controller and a secondary system controller" as recited in Applicant's claim 10. Further, Forsman **does not teach or disclose** "wherein the primary system controller is configured to configure the one or more processors, the one or more memories, and the one or more I/O devices into one or more domains, wherein the primary system controller is further configured to update secondary system controller with a system configuration," as recited in Applicant's claim 10.

Dziadosz is directed toward a computer system having a scaleable software architecture. Applicant can find no reference to a system controller or service processor in Dziadosz.

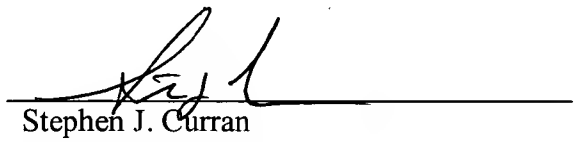
Accordingly, Applicant submits that claim 10, along with its dependent claims, patentably distinguishes over Forsman and over Forsman in view of Dziadosz for the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-51900/SJC.

Respectfully submitted,



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